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EXAMINER	
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ART UNIT	PAPER NUMBER
2651	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/991,557	Applicant(s) VENCA ET AL.	
	Examiner Glenda P. Rodriguez	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-24* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed in by the Applicant on Paper #10, filed 3/8/2004. This rejection is in response to newly found references found by the Examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6, 13-18, 20, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patti et al. (US Patent No. 6, 252, 450) in view of Sedra/Smith ("Microelectronic Circuits", 4th Ed., 1998).

Regarding Claim 1, Patti et al. teach a driver circuit comprising:

Switching circuitry connected between a first voltage supply, a second voltage supply and first and second terminals of the head (Pat. No. 6, 252, 450; Col. 4, Lines 26-36, Col. 5, Lines 18-26 and Col. 7, Lines 3-12. Patti et al. teaches a switching circuitry that is effectuated by transistors in order to control the terminals in the write head (101A and 101B in Fig. 2).);

Timing circuitry connected to the switching circuitry for connecting the first terminal to a first voltage level during a first time period and to a second voltage level during a second time period following the first time period, and connecting the second terminal to a third voltage level during to a first time period and to a

fourth voltage level during a second time period, the first and second time periods occurring when the current through the head transitions between steady state current levels, and the first, second third and fourth voltage levels forming drive signals applied to the head (Pat. No. 6, 252, 450; Col. 4, L. 56-64, Col. 6, L. 41-Col. 7, L. 12 and Col. 8, L. 12-51. Patti et al. teach a sub-circuit for changing currents in the write head that has a control circuitry using pull up devices with delay elements that are supplied into the driver circuit through signals PY, PX, NX and NY switching between 106, 107, 116 and 117, which are current supplying elements. It is obvious to an artisan in the art to know that if a current is being supplied, a voltage is supplied according to Ohm's Law V = IR.).

Patti et al. further teach in Fig. 2 that the sub-circuit 102 is the same as sub-circuit 103 in the driver circuit 100 (See also Col. 2, L. 34-43 in Patti et al.). Patti et al. fails to teach that the drive signals applied are formed into having substantially no common mode voltage. However, this feature is well known in the art as disclosed by Sedra/Smith, wherein it teaches that the output in a common voltage mode configuration (i.e. voltages in both sub-circuits to be the same as in the mathematical relationship $v_{c1} - v_{c2}$ from Fig. 6.10 (b) in page 499) is zero if the circuit on both sides are symmetric (i.e. the same voltage is produced on both sides.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order to have no common voltage in order to protect the circuit from any unwanted output voltage that may damage the circuit (Pat. No. 6, 252, 450; Col. 3, L. 32-48).

Claim 22 has limitations similar to those treated in the above rejection, and is met by the references as discussed above. Claim 22 however also recite the following limitations..." at least one disk on which data is stored (Col. 1, L.9-35); A spindle motor and controller therefore (Fig. 2, Element 130, Patti et al. teach a control CKT element. It is known in the art that the disk is operated by a spindle motor.); A read head (Col. 1, L. 9-17); Read channel circuitry (It is obvious to an artisan of ordinary skill in the art to know that if a read head is coupled to a read channel circuitry in order to acquire the information read back by the read head.); a write head (Col. 1, Lines 61-67).

Claim 24 has limitations similar to those treated in the above rejection(s), and is met by the references as discussed above. Claim 24 however also recite the following limitations..."a plurality of switching transistors (Pat. No. 6, 252, 450; Col. 3, L. 32-48); a plurality of current sources connected between a first voltage supply and second voltage supply (Pat. No. 6, 252, 450; Col. 4, L. 56-64, Col. 6, L. 41- Col. 7, L. 12 and Col. 8, L. 12-51. Patti et al. teach a driver circuit that switches between 106, 107, 116 and 117, which are current supplying elements.)and the minimum pulsewidth appearing on the control signals being an inverse of the rate at which data is written on the disk (Col. 8, L. 10 to Col. 10, L. 10).

Method claim 16 is drawn to the method of using the corresponding apparatus claimed in claim 1. Therefore method claim 16 corresponds to apparatus claim 1 and is rejected for the same reasons of obviousness as used above.

Regarding Claim 2, Patti et al. and Sedra/Smith teach all the limitations of Claim 1. Patti et al. further teach wherein a first current source coupled to the first terminal so as to selectively source a steady state current thereto; and a second current source coupled to the first terminal so

as to selectively sink a steady state current therefrom, the first and second current sources being separately connected to the first terminal via the switching circuitry when the head is in steady state conditions (Pat. No. 6, 252, 450; Col. 5, L. 50 to Col. 6, L. 14).

Regarding Claim 3, Patti et al. and Sedra/Smith teach all the limitations of Claim 2. Patti et al. further teach further comprising: a first current source coupled to the first terminal so as to selectively source a steady state current thereto; and a second current source coupled to the first terminal so as to selectively sink a steady state current therefrom, the first and second current sources being separately connected to the first terminal via the switching circuitry when the head is in steady state conditions (Pat. No. 6, 252, 450; Col. 6, L. 15-29).

Regarding Claim 4 and 18, Patti et al. and Sedra/Smith teach all the limitations of Claims 1 and 16, respectively. Patti et al. further teach wherein the first and fourth voltages are the first voltage supply and the second and third voltages are the second voltage supply (Pat. No. 6, 252, 450; Fig. 2, Elements 106 and 107 are to first voltage and 116 and 117 are to the second voltage.).

Regarding Claim 6, Patti et al. and Sedra/Smith teach all the limitations of Claim 1. Patti et al. further teach wherein the first voltage level is the first voltage supply and the second voltage level is the second voltage supply (Pat. No. 6, 252, 450; Fig. 2, Elements V_{ref1} and V_{ref2} are two voltage supplies used in the driver circuit.).

Regarding Claims 7 and 20, Patti et al. and Sedra/Smith teach all the limitations of Claims 1 and 16, respectively. Patti et al. further teach wherein the first time period is approximately the time it takes for the current flowing through the head to transition from a first

steady state current level to an overshoot current level having a greater magnitude than a second steady state current level (Pat. No. 6, 252, 450; Col. 7, L. 45-65).

Regarding Claim 13, Patti et al. and Sedra/Smith teach all the limitations of Claim 1. Patti et al. further teach a timing circuitry that alternates the voltages between the first and second voltage supply (Pat. No. 6, 252, 450; Col. 4, L. 56-64, Col. 6, L. 41- Col. 7, L. 12 and Col. 8, L. 12-51. Patti et al. teach a control circuitry with delay elements that are supplied into the driver circuit through signals PY, PX, NX and NY switching between 106, 107, 116 and 117, which are current supplying elements.).

Regarding Claim 14, Patti et al. and Sedra/Smith teach all the limitations of Claim 13. Patti et al. further teach wherein the switching circuitry and the timing circuitry selectively provide current paths to the first terminal during the first and second time periods that are in parallel with current paths formed by the first and second current sources (Pat. No. 6, 252, 450; See Fig. 2).

Regarding Claim 15, Patti et al. and Sedra/Smith teach all the limitations of Claim 1. Patti et al. further teach wherein the head is the write head of a disk drive (Pat. No. 6, 252, 450, Fig. 2 and Abstract).

Regarding Claim 17, Patti et al. and Sedra/Smith teach all the limitations of Claim 16. Patti et al. further teach wherein the first and fourth voltages are the same and the second and third voltages are the same (Patti et al. further teach in Fig. 2 that the sub-circuit 102 is the same as sub-circuit 103 in the driver circuit 100 (See also Col. 2, L. 34-43 in Patti et al.), therefore, the voltages are the same.).

Claims 5, 8, 12, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patti et al. and Sedra/Smith as applied to claim 1 above, and further in view of Leighton (US Patent No. 6, 121, 800).

Regarding Claim 5, Patti et al. and Sedra/Smith teach all the limitations of Claim 1. Patti et al. and Sedra/Smith fail to teach wherein the voltage levels are positive and negative supply voltages. However, this feature is well known in the art as disclosed by Leighton et al., wherein it teaches the second and fourth voltage levels are approximately positive and negative supply voltages (Pat. No. 6, 121, 800; Col. 4, Lines 45-60). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order for the driver circuit to take a predetermined time in order to narrow the overshoot pulse and rapid settling to the steady-state write current of the driver.

Regarding Claims 8 and 21, Patti et al. and Sedra/Smith teach all the limitations of Claim 7 and 20, respectively. Patti and Sedra/Smith fail to teach wherein the second time period is approximately the time it takes for the current flowing through the head to transition from the first overshoot current level to an undershoot current level having a lesser magnitude than the second steady state current level. However, this feature is well known in the art as disclosed by Leighton et al., wherein it teaches the second time period is approximately the time it takes for the current flowing through the head to transition from the first overshoot current level to an undershoot current level having a lesser magnitude than the second steady state current level (Pat. No. 6, 121, 800; Col. 2, Lines 7-14.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order for

the driver circuit to take a predetermined time in order to narrow the overshoot pulse and rapid settling to the steady-state write current of the driver.

Regarding Claim 12, Patti et al. and Sedra/Smith teach all the limitations of Claim 1. Patti et al. and Sedra/Smith fail to teach wherein the timing circuitry provides control signals to the switching circuitry, the control signals having a minimum pulse width approximately equal to the reciprocal of the data rate of the memory disk device. However, this feature is well known in the art as disclosed by Leighton et al., wherein it teaches the timing circuitry provides control signals to the switching circuitry, the control signals having a minimum pulse width approximately equal to the reciprocal of the data rate of the memory disk device (Pat. No. 6, 121, 800; Col. 5, Lines 12-32). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order for the driver circuit to take a predetermined time in order to narrow the overshoot pulse and rapid settling to the steady-state write current of the driver.

Regarding Claim 23, Patti et al. and Sedra/Smith teach all the limitations of Claim 22. Patti et al. and Sedra/Smith fail to teach wherein the first and second terminals are connected to opposite supply voltage levels during a first portion of the time a current in the write head transitions between steady state current levels, and the voltage supply levels connected to the first and second terminals are reversed during a second portion of the time the current in the write head transitions between steady state current levels. However, this feature is well known in the art as disclosed by Leighton et al. wherein it teaches that when switching from a first voltage supply to a second voltage supply during a predetermined time periods, the first and second terminals are reversed (Pat. No. 6, 121, 800; Col. 2, Lines 7-14). It would have been

obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Lacombe's invention in order for the driver circuit to take a predetermined time in order to narrow the overshoot pulse and rapid settling to the steady-state write current of the driver.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patti et al. and Sedra/Smith as applied to claim 16 above, and further in view of Lacombe (US Patent No. 6, 400, 190). Patti et al. and Sedra/Smith teach all the limitations of Claim 16. Patti et al. and Sedra/Smith fail to teach wherein the third and fourth voltage levels are approximately at opposite voltage supplies, and the first and second voltage levels have substantially the same magnitude. However, this feature is well known in the art as disclosed by Lacombe, wherein it teaches wherein the third and fourth voltage levels are approximately at opposite voltage supplies, and the first and second voltage levels have substantially the same magnitude (Pat. No. 6, 400, 190; Col. 6, Lines 39-54. Lacombe teaches that the voltages are controlled and can be changed in order to change the current in the coil. It would have been obvious to a person of ordinary skill in the art to be able to then control the voltages with the same magnitude and the first and second voltages opposite in voltage supplies.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order to control the current being supplied to the write head.

Claim 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patti et al. in view of Lacombe et al. (US Patent No. 6, 236, 246).

Regarding Claim 9, Patti et al. teach a driver circuit, comprising:

> Switching circuitry connected between the first voltage supply, a second voltage supply and a first and second terminals of opposite ends of a write coil (Pat. No.

6, 252, 450; See Fig. 2 and Col. 4, Lines 26-36, Col. 5, Lines 18-26 and Col. 7, Lines 3-12. Patti et al. teaches a switching circuitry that is effectuated by transistors in order to control the terminals in the write head (101A and 101B in Fig. 2))

Timing circuitry connected to the switching circuitry for connecting the first terminal to a first voltage level during a first time period and to a second voltage level during a second time period following the first time period, and connecting the second terminal to a third voltage level during to a first time period and to a fourth voltage level during a second time period, the first and second time periods occurring when the current through the head transitions between steady state current levels (Pat. No. 6, 252, 450; Col. 4, L. 56-64, Col. 6, L. 41- Col. 7, L. 12 and Col. 8, L. 12-51. Patti et al. teach a control circuitry with delay elements that are supplied into the driver circuit through signals PY, PX, NX and NY switching between 106, 107, 116 and 117, which are current supplying elements.).

Patti et al. fail to teach wherein a first resistance element connected between the first terminal and a ground reference and a second resistance element connected between the second terminal and the ground reference. However, this feature is well known in the art as disclosed by Leighton et al. ('246), wherein it teaches a first resistance element connected between the first terminal and a ground reference and a second resistance element connected between the second terminal and the ground reference (Pat. No. 6, 236, 246; Fig. 1, Elements R3 and R4). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order to acquire unity of circuit.

Regarding Claim 11, Patti et al. and Leighton et al. ('246) teach all the limitations of Claim 9. Leighton et al. ('246) further teach wherein the first and second resistance elements are disconnected from the first and second terminals, respectively, during the first and second time periods (Pat. No. 6, 236, 246; Fig. 1 and Col. 2, Lines 30-56. Leighton et al. ('246) teaches switching between the nodes 10 and 12. It is obvious that when switching between one node and the other, the resistance elements will also be disconnected.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Patti et al.'s invention in order to acquire unity of circuit.

Allowable Subject Matter

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, alone or inter alia, fail to teach wherein the first and second resistive elements are variable elements.

Response to Arguments

Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection. Claims 1-9 and 11-24 are now rejected in view of Patti et al. in view of Sedra/Smith.

Regarding Applicants arguments for Claim 9, Examiner cannot concur because the Claim 9 fails does not recite the argument made by the Applicant in Paper #10, Page 11, L. 7-15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703)305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703)308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
May 18, 2004.

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